IN THE CLAIMS:

Please amend the claims as follows. All of the claims are reproduced below for the Examiner's convenience. A marked up version of the amended claims is provided as an attachment.

1.   (Amended) A media processing system, comprising:

DRAM having a plurality of storage locations for storing digital data being processed by said media processing system, said digital data including video data that is compressed in a first standardized format;

means for processing said digital data that includes said first standardized format compressed video data to produce compressed video images and image data;

means for decoding said first standardized format compressed video images to generate full motion video pixel data;

means for sharing said DRAM between said processing means and said decoding means; and

means for producing a full motion video signal from said full motion video pixel data;

wherein the means for decoding the first standardized format compressed video images is adapted for reconfiguration to decode digital data including data that is compressed in a second standardized format.

2.   (Amended) The system as recited in claim 1, wherein said compressed video data comprises a plurality of pixels, and said first standardized compressed format comprises a luminance sample generated for each pixel, and two chrominance samples generated for every four pixels.

3.   The system as recited in claim 2, wherein said decoding means comprises a Motion Picture Expert Group decoder.

4.   The system as recited in claim 1, wherein said compressed video data comprises a plurality of pixels, and said processing means comprises means for multiplying a first pixel with a second pixel in a single clock cycle of said processing means.

5.   The system as recited in claim 4, wherein said pixels have a first portion, a second portion and a third portion, and said means for multiplying pixels comprises means for multiplying a portion of the first pixel with a corresponding portion of the second pixel.

6.   The system as recited in claim 1, wherein said compressed video data comprises a plurality of pixels, and said processing means comprises means for combining a first pixel with a second pixel in a single clock cycle of said processing means.

7.   The system as recited in claim 6, wherein said pixels have a first portion, a second portion and a third portion, and said means for combining pixels comprises means for combining a portion of the first pixel with a corresponding portion of the second pixel.

8.   The system as recited in claim 1, wherein said processing means comprises a plurality of processing elements connected together in parallel, means for controlling said processing elements with instruction words that have a predetermined number of instructions, and means for distributing data simultaneously to each of said processing elements.

9.	The system as recited in claim 8, wherein said processing elements comprise a plurality of processing units wherein each of said processing units is controlled by one of said predetermined number of instructions.

10.	(Amended) The system as recited in claim 1, wherein said DRAM stores audio data that is compressed in a standardized format, and further comprising means for decompressing said audio data that is compressed in a first standardized format to generate uncompressed audio data, and means for combining said full-motion video data and said uncompressed audio data to generate full-motion multimedia data.

11.	The system as recited in claim 9, wherein said processing units comprise a plurality of storage locations within said processing units, each storage location having a predetermined physical size, and means for combining said storage locations together to form a storage location that stores data that is larger than the predetermined physical size of each storage location.

12.	(Amended) A single semiconductor chip media processor, comprising:

a semiconductor memory, internal to said single semiconductor chip, for storing digital data, including video digital data compressed in first standardized format;

means for processing said compressed video data in said semiconductor memory to produce color, full motion video data that is temporarily stored in said semiconductor memory;

means for decoding said color, full motion video data stored in said semiconductor memory to generate color, full motion video image data; and

means for producing a color, full motion video image signal;

wherein the means for decoding said color, full motion video data is adapted for reconfiguration to decode video data compressed in a second standardized format.

13. (Amended) The processor as recited in claim 12, wherein said first compressed video data comprises a plurality of pixels, and said processing means comprises means for multiplying a first pixel with a second pixel in a single clock cycle of said processing means.

14. The processor as recited in claim 13, wherein said pixels have a first portion, a second portion and a third portion, and said means for multiplying pixels comprises means for multiplying a portion of the first pixel with a corresponding portion of the second pixel.

15. The processor as recited in claim 14, wherein said compressed video data comprises a plurality of pixels, and said processing means comprises means for combining a first pixel with a second pixel in a single clock cycle of said processing means.

16. The processor as recited in claim 15, wherein said pixels have a first portion, a second portion and a third portion, and said means for combining pixels comprises means for combining a portion of the first pixel with a corresponding portion of the second pixel.

17. The processor as recited in claim 12, wherein said processing means comprises a plurality of processing elements connected together in parallel, means for controlling said processing elements with instruction words that have a predetermined number of instructions, and means for distributing data simultaneously to each of said processing elements.

18.　The processor as recited in claim 17, wherein said processing elements comprise a plurality of processing units wherein each of said processing units is controlled by one of said predetermined number of instructions.

19.　(Amended) The processor as recited in claim 12, wherein said DRAM stores audio data that is compressed in a first standardized format, and further comprising means for decompressing said audio data that is compressed in the first standardized format to generate uncompressed audio data, and means for combining said full-motion video data and said uncompressed audio data to generate full-motion multimedia data.

20.　The processor as recited in claim 18, wherein said processing units comprise a plurality of storage locations within said processing units, each storage location having a predetermined physical size, and means for combining said storage locations together to form a storage location that stores data that is larger than the predetermined physical size of each storage location.

21.　(Amended) A method of processing media, comprising:

storing digital data being processed by said media processing system in a DRAM, said digital data including video data that is compressed in a first standardized format;

processing said digital data that includes said first standardized format compressed video data to produce compressed video images and image data;

decoding said first standardized format compressed video images to generate full motion video pixel data;

sharing said DRAM between said processing means and said decoding means;

producing a full motion video signal from said full motion video pixel data; and

decoding video images compressed in a second standardized format to generate full motion video pixel data.

22.   The method as recited in claim 20, wherein said compressed video data comprises a plurality of pixels, and processing comprises multiplying a first pixel with a second pixel in a single clock cycle.

23.   The method as recited in claim 21, wherein said compressed video data comprises a plurality of pixels, and processing comprises combining a first pixel with a second pixel in a single clock cycle.

24.   (New) A media processing system, comprising:

an arrangement configured to receive digital information, the digital information including video data and control commands;

a plurality of processors configured to process the video data in response to the control commands;

a first arrangement configured to transport the control commands among the plurality of processors; and

a second arrangement configured to transport portions of the data among the plurality of processors;

wherein the plurality of processors cooperate to produce full-motion color images.

25.   (New) The system recited in claim 24, wherein the digital data includes video data that is compressed in a standardized format.